SIR Endec for IrDA Applications Integrated Interface Circuit

Description

The TOIM5232 Endec IC provides proper pulse shaping for the SIR IrDA® front end infrared transceivers as of the 4000-series.
For transmitting the TOIM5232 shortens the RS232 output signal to IrDA compatible electrical pulses to drive the infrared transmitter. In the receive mode, the TOIM5232 stretches the received infrared pulses to the proper bit width depending on the operating bit rate. The IrDA bit rate varies from 2.4 kbit/s to 115.2 kbit/s.
The TOIM5232 is using a crystal clock 3.6864 MHz (< 7.5 MHz) for its pulse stretching and shortening. The clock is generated by the internal oscillator. An external clock can be used, too. The TOIM5232 is programmable to operate from 1200 bit/s to 115.2 kbit/s by the communication software through the RS232 port. The output pulses are software programmable as either 1.627 µs or 3/16 of bit time. The typical power consumption is very low with about 10 mW in operational state and in the order of a few microwatts in standby mode. TOIM5232 in the tiny QFN-20 package is the space-minimized version of TOIM5232.

ULC Technology: High performance gate array package using multiple metal layer CMOS technology featuring sub-micron channel lengths (0.35 µm).

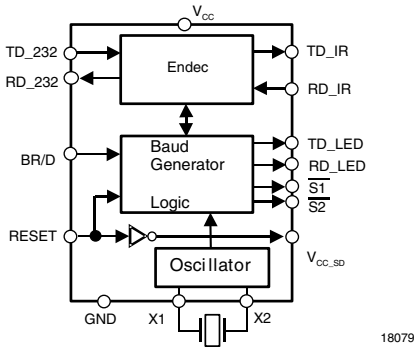
Features

- Pulse shaping function according IrDA SIR physical layer
- Directly interfaces the SIR transceiver to an RS232 port
- QFN-20 - package, 4 mm x 4 mm x 0.75 mm
- Low operating current
- Programmable baud clock generator (1200 Hz to 115.2 kHz), 13 baud rates
- 3/16 bit pulse duration or 1.627 µs pulse selectable
- For 2.7 V to 3.6 V operation voltage, 5 V tolerant inputs
- Lead (Pb)-free device
- Qualified for lead (Pb)-free and Sn/Pb solder processing (MSL3)
- Device in accordance with RoHS 2002/95/EC and WEEE 2002/96EC

Ordering Information

Part number	Qty/reel
TOIM5232-TR3	6000 pcs

Block Diagram



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Pin Assignment and Description

Pin number	Symbol	Function	I/O	Active
1	RD_232	Received signal data output of stretched signal to the RS232 RXD line (using level converter).	O	High
2	TD_232	Input of the signal to be transmitted from the RS232 port TXD line (passing the level converter).	I	High
3	V_{CC_SD}	This pin can be used to shut down a transceiver (e.g., TFDx4xxx). Output polarity: Inverted RESET input.	O	Low
4	X1	Crystal input clock, 3.6864 MHz nominal for 9.6 kbit/s default setting. Input for external clock[1]. Option: 7.3728 MHz for 19.2 kbit/s default operation.	I	
5	X2	Crystal[1]	I	
7	GND	Ground in common with the RS232 port and IrDA transceiver ground		
9	TD_LED	Transmit LED indicator driver. Use 180 Ω current limiting resistor in series to LED to connect to V_{CC} (V_{CC} = 3.3 V).	O	Low
10	RD_LED	Receive LED indicator driver. Use 180 Ω current limiting resistor in series to LED to connect to V_{CC} (V_{CC} = 3.3 V).	O	Low
12	S1	User programmable bit. Can be used to turn ON/OFF a front-end infrared transceiver (e.g., an infrared module at the adapter front).	O	Low
13	S2	User programmable bit. Can be used to turn ON/OFF a front-end infrared transceiver (e.g., an infrared module at the adapter back).	O	Low
14	TD_IR	Data output of shortened signal to the infrared transceiver.	O	High
16	RD_IR	Data input from the infrared transceiver, min. pulse duration 1.63 µs [2]	I	Low
17	V_{CC}	Supply voltage	I	
18	RESET	Resets all internal registers. Initially must be HIGH ("1") to reset internal registers. When HIGH, the TOIM5232 sets the IrDA default bit rate of 9600 bit/s, sets pulse width to 1.627 µs. The V_{CC_SD} output is simply an inverted reset signal which allows shutdown of a TFDx4x00 transceiver when applying the reset signal to the TOIM5232. When using devices with external SD like TFDU4203, the reset line can be used directly as shut down signal. RESET pin can be controlled by either the RTS or DTR line through RS232 level converter. Minimum hold time for resetting is 1 µs. **Disables the oscillator when active.**		High
19	BR/D	**Baud rate control/data** **BR/D = 0, data communication mode:** RS232 TXD data line is connected (via a level shifter) to TD_232 input pin. The TXD - signal is appropriately shortened and applied to the output TD_IR, driving the TXD input of the IR transceiver. The RXD line of the transceiver is connected to the RD_IR input. This signal is stretched to the correct bit length according to the programmed bit rate and is routed to the RS232 RXD line at the RD_232 pin. **BR/D = 1, programming mode:** Data received from the RS232 port is interpreted as control word. The control word programs the baud rate width will be effective as soon as BR/D return to LOW.		
6, 8, 11, 15, 20		NC		

Note:

1) Crystal should be connected as shown in the block diagram or in the recommended application circuit. Connect a 100 kΩ resistor from pin 4 to pin 5 and from pin 4 and pin 5 a 22 pF capacitor to ground, respectively. When an external clock is available connect it to pin 4 leaving pin 5 open. The external resistor of 100 kΩ is used to accelerate the start of the oscillation after reset or power-on. The value depends on the "Q" of the resonator. With low Q resonators no resistor is needed. The start-up time of the oscillator is between 30 µs (with piezo resonators) and above 2 ms with high Q quartzes.
2) This condition is fulfilled with all Vishay IR transceivers.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage	V_{CC}	- 0.5		3.6	V	
Input voltage		- 0.5		5.5	V	All pins
Output voltage		- 0.5		V_{CC} + 0.5	V	All pins
Output sinking current	I_{OUT}	8			mA	All pins
Junction temperature	T_J			125	°C	
Ambient temperature (operating)	T_{amb}	- 25		85	°C	
Storage temperature	T_{stg}	- 25		85	°C	
Soldering temperature	T_{sldr}			260	°C	

DC Characteristics

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Operating voltage		V_{CC}	2.7	3.3	3.6	V
V_{CC} = 3.3 V ± 5 %, operating temperature = - 25 °C to + 85 °C						
Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Input HIGH voltage	Inputs tolerate levels as high as 5.5 V max. All inputs are Schmitt trigger inputs	V_{IH}	2.0			V
Input LOW voltage		V_{IL}			0.8	V
Input Schmitt trigger hysteresis		V_{hyst}		0.6		V
Input leakage no pull-up/down	V_{IN} = V_{CC} or GND	I_L	- 10	± 1	10	µA
Output HIGH voltage	I_{OH} = - 2.0 mA	V_{OH}	2.0			V
	I_{OH} = - 0.5 mA	V_{OH}	2.4			V
Output LOW voltage	I_{OL} = + 2.0 mA	V_{OL}			0.4	V
Consumption current standby	Inputs grounded, no output load V_{CC} = 3.3 V, T = 25 °C	I_{SB}			1	µA
Consumption current dynamic	Inputs grounded, no output load V_{CC} = 3.3 V, T = 25 °C	I_{CC}		2		mA

Operation Description

The block diagram shows a typical example of an RS232 port interface. The TOIM5232 connects to an RS232 level converter on one side, and an infrared transceiver on the other. The internal TOIM5232 baud rate generator can be software controlled.

When BR/D = 0, the TOIM5232 interprets the channels TD_232 to TD_IR and RD_IR to RD_232 as data channels.

On the other hand, whenever BR/D = 1, the TOIM5232 interprets TD_232 as control word for setting the baud rate. The baud rate can be programmed to operate from 1200 bit/s to 115.2 kbit/s. As RS232 level converter, EIA232 or MAX232 or equivalent are recommended.

When using the TOIM5232 directly connected to an UART it is compatible to 5 V TTL and 3.3 V CMOS logic.

Typical external resistors and capacitors are needed as shown in the TFDU4.../TFBS4...-series references.

The output pulse duration can also be programmed, see chapter "Operation Description". It is strongly recommended using 1.627 µs output pulses to save battery power. As frequency determining component a Vishay XT49M Crystal is recommended, when no external clock is available.

We strongly recommend not to use this 3/16 mode because 3/16 pulse length at lower bit rates consumes more power than the shorter pulse. At a data rate of 9600 bit/s, the ratio of power consumption of both modes is a factor of 12 (!).

Programming the TOIM5232

For correct data rate dependent timing the TOIM5232 is using a built-in baud rate generator. This is used when no external clock is not available as in RS232 IR-dongle applications. For programming the BR/D pin has to be set active, BR/D = 1.

In this case the TOIM5232 interprets the 7 LSBs at the TD_232 input as a control word. The operating baud rate will change to its supposedly new baud rate when the BR/D returns back to LOW ("0") Set the UART to 8 bit, no parity, 1 stop bit.

Control Byte (8 bit)

First character				Second character			
X	S2	S1	S0	B3	B2	B1	B0
							LSB

X: Do not care
S1, S2: User programmable bit to program the outputs S1 and S2
S0: Irda pulse select
S0 = (1): 1.627 µs output pulses
S0 = (0): 3/16 bit time pulses, not recommended
B0 to B3: Baud rate select words according following table.

Example:
To set TOIM5232 at COM2 port (2F8) to 9600 bit/s with 3/16 bit time pulse duration send to the TOIM5232 in programming mode in e.g. "Basic"
OUT &H2F8, (&H6)
For same port, 9600 bit/s and 1.627 µs pulse duration send
OUT &H2F8, (&H16)
For additionally activating S1 send
OUT &H2F8, (&H36)

Baud Rate Select Words

B3	B2	B1	B0	2nd char	Baud rate
0	0	0	0	0	115.2 k
0	0	0	1	1	57.6 k
0	0	1	0	2	38.4 k
0	0	1	1	3	19.2 k
0	1	0	0	4	14.4 k
0	1	0	1	5	12.8 k
0	1	1	0	6	9.6 k
0	1	1	1	7	7.2 k
1	0	0	0	8	4.8 k
1	0	0	1	9	3.6 k
1	0	1	0	A	2.4 k
1	0	1	1	B	1.8 k
1	1	0	0	C	1.2 k

Note:
IrDA standard only supports 2.4 kbit/s, 9.6 kbit/s, 19.2 kbit/s, 57.6 kbit/s, and 115.2 kbit/s (3.6864 MHz clock). Doubling the baud rates is allowed by doubling the clock frequency.

Software for the TOIM4232 and TOIM5232 UART Programming

For proper operation, the RS232 must be programmed (using 8 bit, 1 stop, no parity) to send a two character control word, YZ. The control word YZ is composed of two characters, written in hexadecimal, in format: YZ. The transfer rate for programming must be identical with the formerly programmed data rate, or after resetting the TOIM5232, the default rate of 9600 bit/s is used.

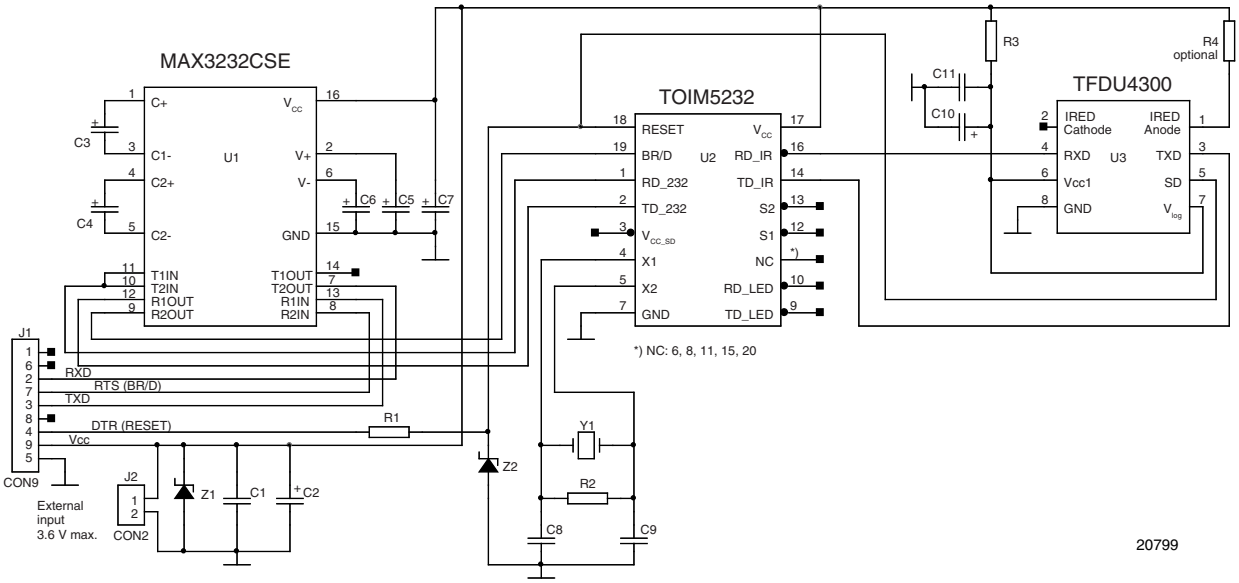
Step.	RESET	BR/D	TD_UART	RD_UART	RD_IR	TD_IR	Description and comments
1	High	X	X	X	X	X	Resets all internal registers. Resets to IrDA default data rate of 9600 bit/s
2	Low	X	X	X	X	X	Wait at least 2 ms, to allow start-up of internal clock. When external clock is used: Wait at least 7 µs.
3	Low	High	X	X	X	X	Wait at least 7 µs. TOIM5232 now is set to the control word programming mode
4	Low	High	YZ with Y = 1: 1.627 µs Y = 0 3/16 bit length	X	X	X	Sending the control word YZ. Examples: Send "1Z" if 1.627 µs pulses are intended to be used. Otherwise send "0Z" for 3/16 bit period pulses. "Y6" keeps the 9.6 kbit/s data rate. Z = 0 sets to 115.2 kbit/s, see programming table. Wait at least 1 µs for hold-time.
5	Low	Low	Data	Data	Data	Data	With BR/D = 0, TOIM5232 is in the data communication mode. Both RESET and BR/D must be kept LOW ("0") during data transmission. Reprogramming to a new data rate can be resumed by restarting from step 3. The UART itself also must set to the correct data rate[1)].

Note:

1) For programming the UART, refer to e.g., National Semiconductors data sheet of PC 16550 UART

It is recommended reading the I/O buffer after transmission waiting the specified latency allowance. That avoids receiving unexpected data from pulses stochastically generated by many transceivers during the latency time.

Recommended Application Circuit for TOIM5232



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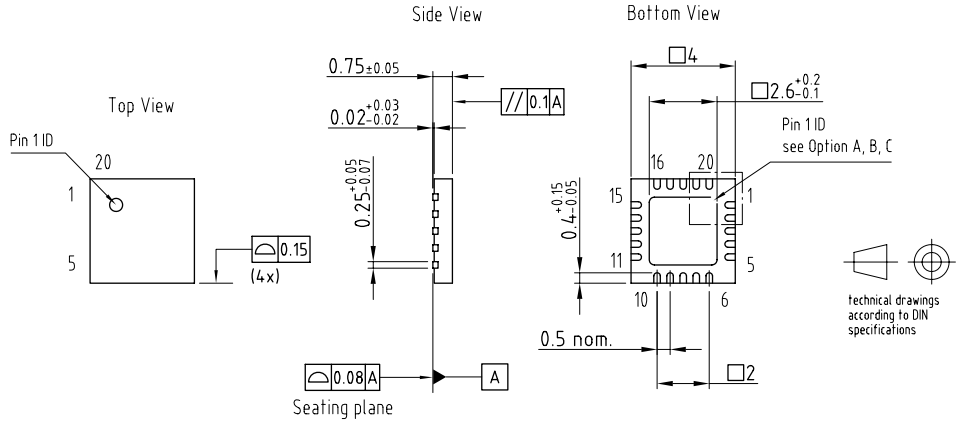
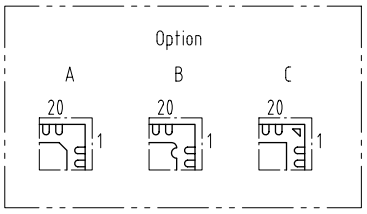
Application circuit using TFDU4300 with integrated level shifter MAX3232CSE. When used directly with 3 V - or 5 V - logic, the level shifter can be omitted.

Recommended Application Circuit Components

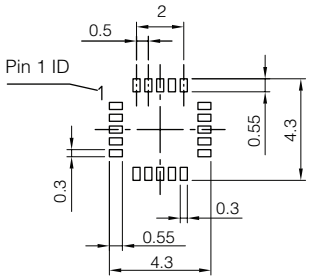
	Component	Recommended value	Vishay part number
1.	C1	100 nF	VJ 1206 Y 104 J XXMT
2.	C2	10 µF, 16 V	293D 106X9 016B 2T
3.	C3	100 nF	VJ 1206 Y 104 J XXMT
4.	C4	100 nF	VJ 1206 Y 104 J XXMT
5.	C5	100 nF	VJ 1206 Y 104 J XXMT
6.	C6	100 nF	VJ 1206 Y 104 J XXMT
7.	C7	1 µF, 16 V	293D 105X9 016A 2T
8.	C8	22 pF	VJ 1206 A 220 J XAMT
9.	C9	22 pF	VJ 1206 A 220 J XAMT
10.	C10	6.8 µF, 16 V (optional)	293D 685X9 016B 2T
11.	C11	100 nF	VJ 1206 Y 104 J XXMT
12.	Z1	3.6 V	BZT55C3V6
13.	Z2	3.6 V	BZT55C3V6
14.	R1	5.6 kΩ	CRCW-1206-5601-F-RT1
15.	R2	100 kΩ	CRCW-1206-1003-F-RT1
16.	R3	47 Ω	CRCW-1206-47R0-F-RT1
17.	R4	27 Ω (for reduced current only)	CRCW-1206-27R0-F-RT1
18.	Y1	3.686400 MHz	XT49S - 20 - 3.686400M
19.	U1	MAX 3232CSE	MAXIM MAX 3232CSE
20.	U2		TOIM5232
21.	U3		TFDU4300
22.	J1	9 pin - connector	Cannon
23.	J2	Power connector	Philmore PHI 211B

Package Dimensions in mm





Recommanded footprint



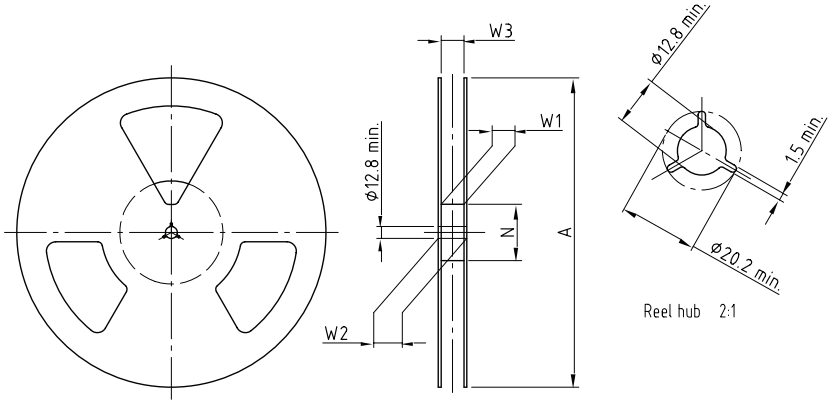
Drawing refers to following types:
TOIM5232 in QFN_4x4_20L, Exposed pad 2.6x2.6
(Compliant JEDEC STANDARD MO-220 variation WGGD-5)

Drawing-No.: 6.543-5146.01-4

Issue: 1; 13.07.07

20797

Reel Dimensions in mm



Drawing-No.: 9.800-5090.01-4
Issue: 1; 29.11.05

14017

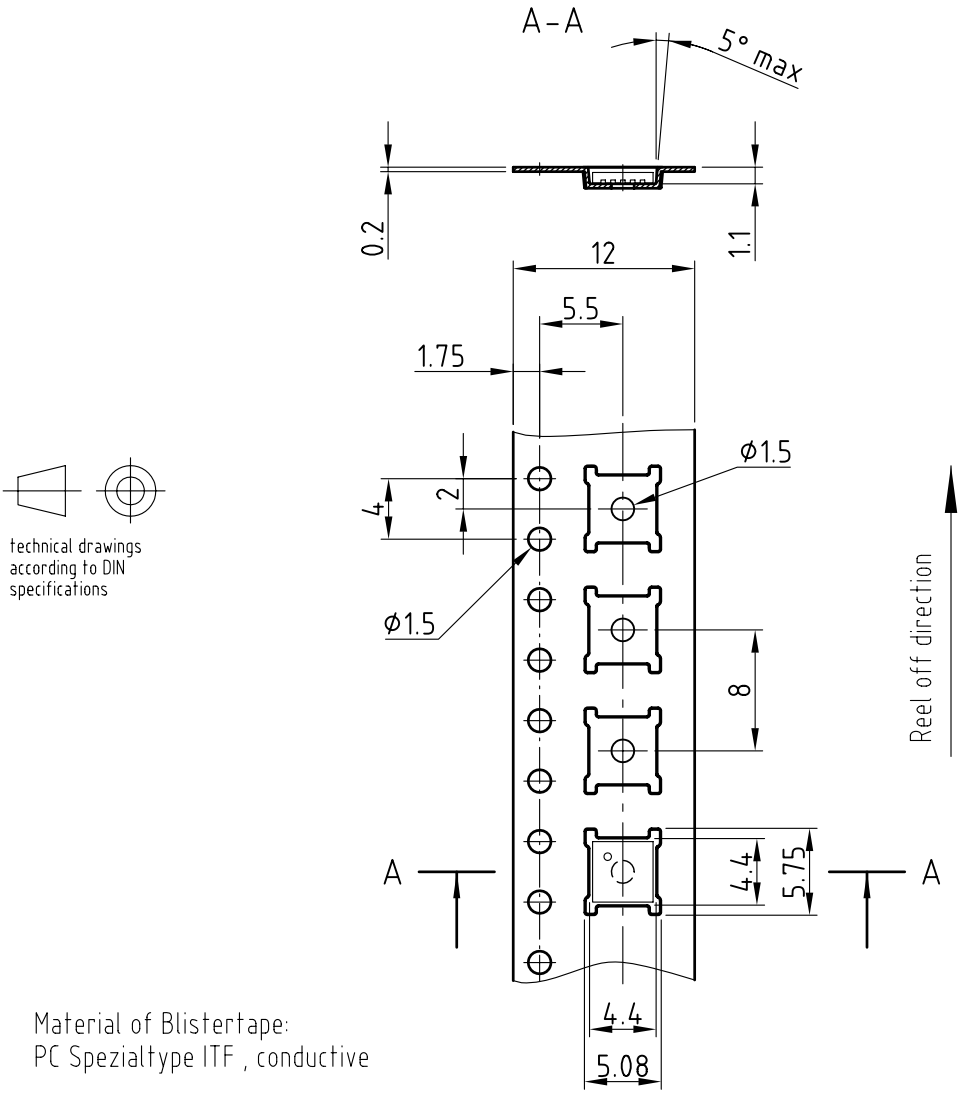
Form of the leave open
of the wheel is supplier specific.

Dimension acc. to IEC EN 60 286-3

technical drawings
according to DIN
specifications

Tape width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
12	330	50	12.4	22.4	11.9	15.4

Tape Dimensions in mm



Material of Blistertape:
PC Spezialtype ITF , conductive

Drawing-No.: 9.700-5327.01-4
Issue: 1; 13.07.07

20798

TOIM4232 (TOIM5232) Encoder - Decoder Interface Programming and Data Transmission

Operation and programming of the TOIM4232 and TOIM5232 interface devices are described below. Figure 1 shows the basic circuit design with 3 blocks: the RS232 to 3-V logic level shifter, the Encoder/ Decoder (Endec) circuit and the transceiver to build a dongle for RS232 IrDA extension. U1 is the level shifter to convert the RS232 logic levels to unipolar 3-V logic; U2 is the Encoder/Decoder Interface (Endec) converting the NRZ - RS232 logic to IrDA RZI - logic. The transceiver U3 transmits and receives IrDA-compliant optical signals.

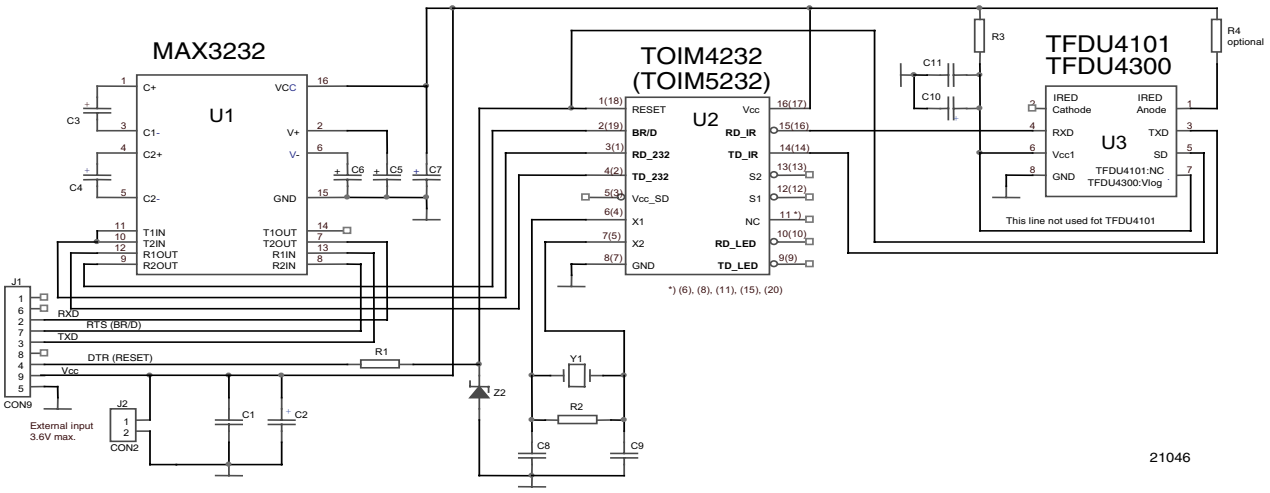


Figure 1. Circuit Diagram of the Demo Board

Circuit Description

This circuit demonstrates the operation of an SIR IrDA transceiver module. The transceiver U3 (e.g., as shown the TFDU4101 or TFDU4300 or any other) converts the digital electrical input signal to an optical output signal to be transmitted, receives the optical signal, and converts these to electrical digital signals. While the IrDA physical layer protocol transmits only the “0” represented by a pulse with a “Return to Zero Inverted (RZI)” logic, the RS232 protocol needs a “No Return to Zero (NRZ)” representation. This decoding/ encoding process is done by U2, an interface circuit stretching the received pulses and shortening the pulses to be transmitted according to the IrDA physical layer conditions. U1 interfaces the RS232 logic bipolar levels to the 3-V logic of the Endec U2. The board is connected by CON9 to the RS232 port (of a computer or other equipment. The basic IrDA transmission speed is 9600 bit/s. This is the default state of the Endec in power-on condition. Also, activating the reset line at pin 1 (18) will set the device to this basic state.

Note: The first pin number refers to TOIM4232; the second number in brackets refers to TOIM5232. The crystal Y1 controls the timing of the Endec as a clock reference. The outputs S1 and S2 are programmable outputs for control operations and the outputs RD_LED and TD_LED can drive LEDs for indicating data flow.

Programming the Endec

For decoding data rates other than the default, the Endec is to be programmed to set the internal counters and timers. To switch the Endec from the Data transfer mode to the Bit Rate programming mode, the input BR/D, pin 2 (19) is set active high (BR/D = “1”). In this case the TOIM5232 interprets the 7 LSBs at the TD_232 input as a control word. The operating bit rate will change to its supposedly new rate when the BR/D returns back to LOW (“0”). Set the UART to 8 bit, no parity, 1 stop bit.

The control byte consists of 8 bit after the start bit (STA, which is “0”). Keep in mind that the order is LSB first, MSB last.

The diagram in figure 2 shows the programming byte **"0-1010-1100"** in the order
STA, B0, B1, B2, B3, S0, S1, S2, X. This order is from right to left in table 1. B0 is sent first as LSB (see figure 2).
The four least significant bits are responsible for the data rate according to table 2 while the four higher bits are for setting the IrDA pulse duration (S0), and the two outputs of the Endec S1 and S2. Bit 8 is not used.

Control Byte (8 bit)

First character				Second character				STA
X	S2	S1	S0	B3	B2	B1	B0	0
MSB							LSB	
Example								
0	0	1	1	0	1	0	1	0
In the oscilloscope that will be shown in the reserved order with LSB first, see figure 2.								
STA	First character				Second character			
0	B0	B1	B2	B3	S0	S1	S2	X
	LSB							MSB
Example								
0	1	0	1	0	1	1	0	0

Table 1

X: Do not care

S1, S2: User-programmable bit to program the outputs S1 and S2. In the example, S1 is set active, and S2 is inactive.

S0: IrDA pulse select

S0 = (1): 1.627 µs output

S0 = (0): 3/16 bit time pulses, not recommended

B0 to B3: Baud rate select words according to the following table 2 below.

Transmission rate select words					
B3	B2	B1	B0	hex	Bit rate
0	0	0	0	0	115.2 k
0	0	0	1	1	57.6 k
0	0	1	0	2	38.4 k
0	0	1	1	3	19.2 k
0	1	0	0	4	14.4 k
0	**1**	**0**	**1**	**5**	**12.8 k**
0	1	1	0	6	9.6 k
0	1	1	1	7	7.2 k
1	0	0	0	8	4.8 k
1	0	0	1	9	3.6 k
1	0	1	0	A	2.4 k
1	0	1	1	B	1.8 k
1	1	0	0	C	1.2 k

Table 2

Bold: See example

Note:

IrDA standard only supports 2.4 kbit/s, 9.6 kbit/s, 19.2 kbit/s, 57.6 kbit/s, and 115.2 kbit/s (3.6864 MHz clock). Doubling the baud rates is permissible by doubling the clock frequency.

In figure 2 the programming sequence is shown for a bit rate of 12.8 kbit/s.

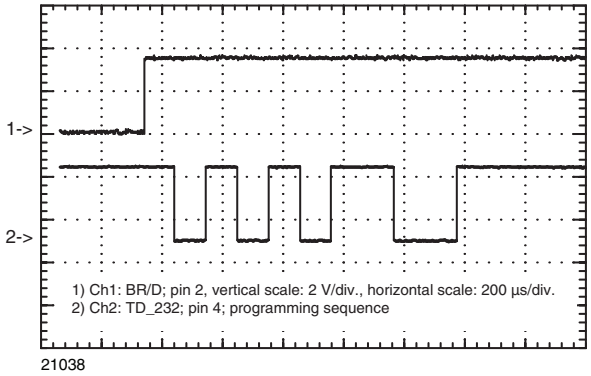


Figure 2.
Programming sequence for setting the Endec to a bit rate of 12.8 kbit/s. After setting BR/D high (Ch1), the programming sequence with the control byte (Ch2) is applied to TD_232, pin 4.

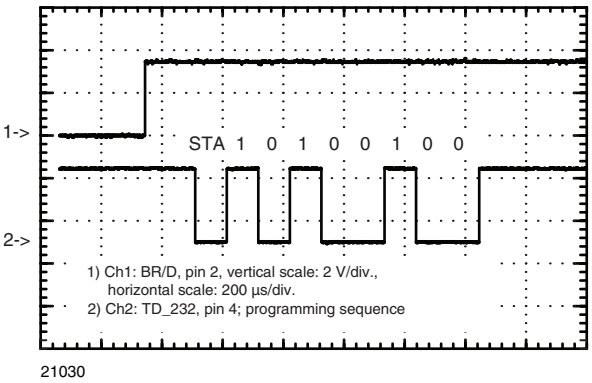


Figure 3.
Programming sequence for setting the Endec to a bit rate of 12.8 kbit/s as in figure 2 but with a 3/16 bit pulse duration (S0 = "0").

Example								
0	0	1	0	**0**	1	0	1	0
MSB							LSB	STA

When correctly programmed, the Endec shortens the pulse to be transmitted from the full bit duration to either 3/16 of the bit length or to 1.627 µs (which is 3/16 of the 115.2 kbit/s bit duration). For power saving, the short pulse is recommended.
The received optical pulse shows in case of most of the VISHAY SIR transceivers, constant pulse duration. The Endec stretches that to the correct bit time according the bit rate setting. This is shown in the following chapters.

Transmit (TXD) Channel

Figure 4 shows the transmission in the default mode. For data transfer, the Endec is set to that mode by BR/D = “0”. In the examples "6" is always transmitted (binary “00000110”). The “0” is represented in the IrDA protocol by an optical pulse. Also here the LSB is transmitted first after the start bit. “1” is not transmitted.

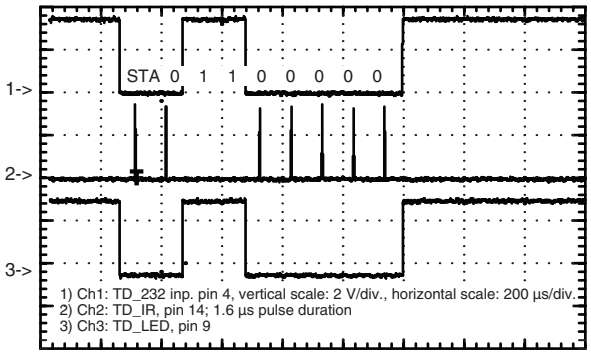


Figure 4. Data transmission with 9.6 kbit/s, 1.627 µs pulse duration

Channel 1 shows the signal from the RS232 port already converted to 3-V logic by U1. The Endec encodes that signal to the RZI IrDA format where a “0” is represented by a pulse. That is the trace of channel 2. This output is connected the TXD input of the transceiver and this signal is transmitted as optical output signal. Channel 3 is the signal for an indicator lamp connected to the TD_LED driver output. Use 180 Ω serial resistor to supply voltage for limiting the current through the LED (not shown in the circuit diagram).

When using the (not recommended) 3/16-bit pulse width the oscillogram looks like figure 5.

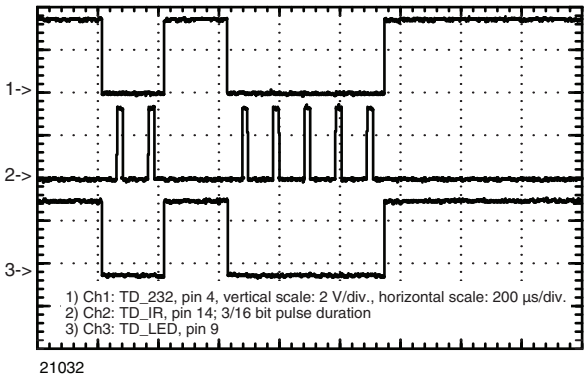


Figure 5. Data transmission with the setting 9.6 kbit/s, 3/16 bit pulse duration (19.5 µs)

The transmission with the highest SIR bit rate of 115.2 bit/s looks like what is shown in figure 6. However, the horizontal time scale is different.

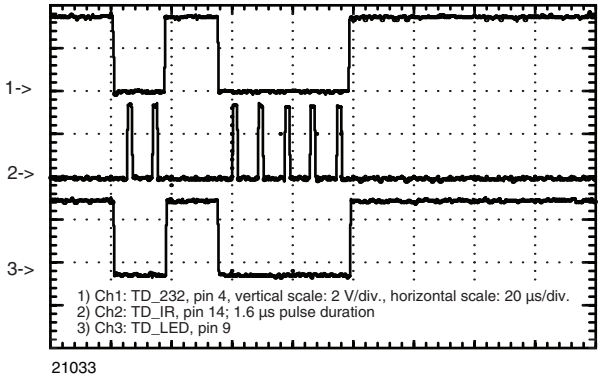


Figure 6. Data transmission with the setting 115.2 kbit/s, 1.627 µs pulse duration. By definition, the pulse duration of 1.627 µs is identical to the 3/16-bit pulse width.

Receive (RXD) Channel

In the default 9600 bit/s mode the signals will look like those shown in figure 7 and figure 8.

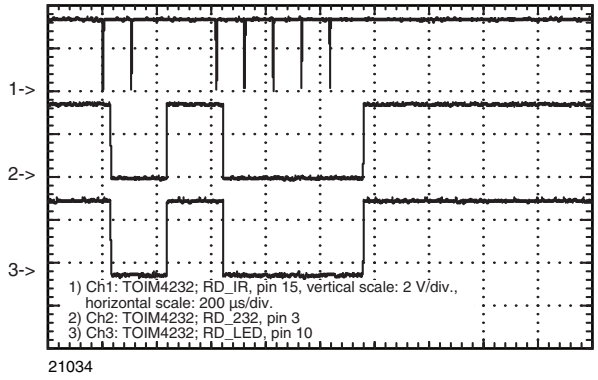


Figure 7. Data reception with the setting 9.6 kbit/s. Short RXD pulse

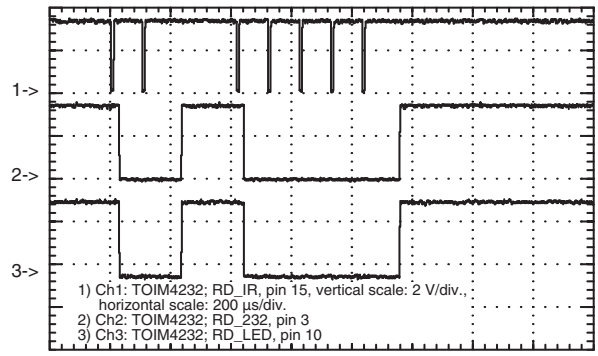


Figure 8. Data reception with the setting 9.6 kbit/s.
Same as in figure 7, extended pulse duration

The Endec stretches the received pulses of about 2 µs duration from the transceiver output (figure 7, channel 1) independent of the pulse duration to the full bit width generating NRZ code (channel 2). Channel 3 is the signal for the indicator lamp.
As shown in figure 8, channels 2 and 3, the final NRZ signal is identical to figure 7, even when longer pulses are received.
In the 115.2 kbit/s mode the signals will look like those shown in figure 7 and figure 8. The difference is just the time scale. It also indicates the delay of the decoded channel 2 vs. channel 1.

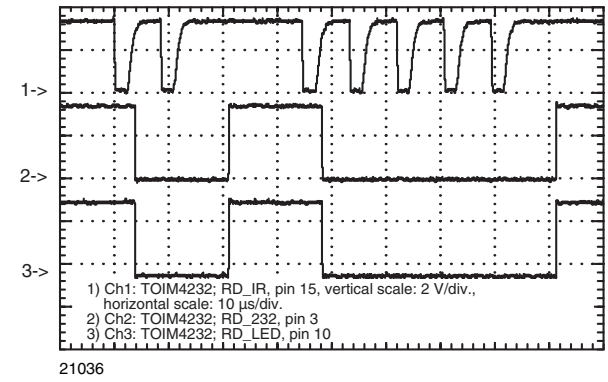


Figure 9. Data reception with the setting 115.2 kbit/s

Channel 1 shows the signal from the transceiver. In this case it is TFDU4100 with unsymmetrical switching times. TFDU4100 (obsolete) used an open collector output with an internal load resistor. That caused a slow trailing edge (but fast enough for all applications). The later generations are using tri-state outputs with push-pull drivers with symmetrical pulse switching times. All VISHAY IrDA transceivers exhibit constant output pulse duration in SIR mode of about 2 µs independent of the duration of the optical input pulse.

“Echo-on" or "Echo-off" and "Latency Allowance”

During transmission, the receiver inside a transceiver package is exposed to very strong irradiance of the transmitter, which causes overload conditions in the receiver circuit. After transmission it takes some time to recover from this condition and return to the specified sensitivity.
During this time the receiver is in an unstable condition, and at the output unexpected signals may arise. Also, during transmission under overload conditions the receiver may show signals on the RXD channel that are similar to or identical with the transmitted signal. To get clean or at least specified conditions for the receive channel during transmission, different terms were defined. The time to allow the receiver to recover from overload conditions is the latency allowance or shorter, just the specified latency. This is covered by the IrDA physical layer specification and is a maximum of 10 ms. IrDA specifies shorter negotiable latency. In SIR the minimum is 0.5 ms. This includes software latency. Transceivers are in general below 0.3 ms.
In the first generations, some suppliers did not care for the behavior of the RXD output of the transceivers during transmission and latency time. The software is able to handle that. The easiest way is to clean up the receiver channel after sending the last pulse and waiting for the latency period.
Later, many transceivers that block the RXD channel during transmission and during the latency period were released to the market. This behavior is called “Echo-off”. Unfortunately, some OEMs like to use the signal from the RXD channel during transmission, as a self-test feature for testing the device on board without using the optical domain. Therefore, many new devices have been developed to echo the TXD input signal at the RXD output. Such behavior is called “echo-on”.
Some software developed for “echo-off” applications is not able to receive and understand the signals from echo-on devices correctly.
Therefore, an add-on to the circuit shown in figure 1 was generated to suppress the echo from the receiver during transmission. This modification is shown in figure 10.
During transmission, the signal from the RXD output of the transceiver is just gated by the transmit signal, (see the oscilloscope picture in figure 11).

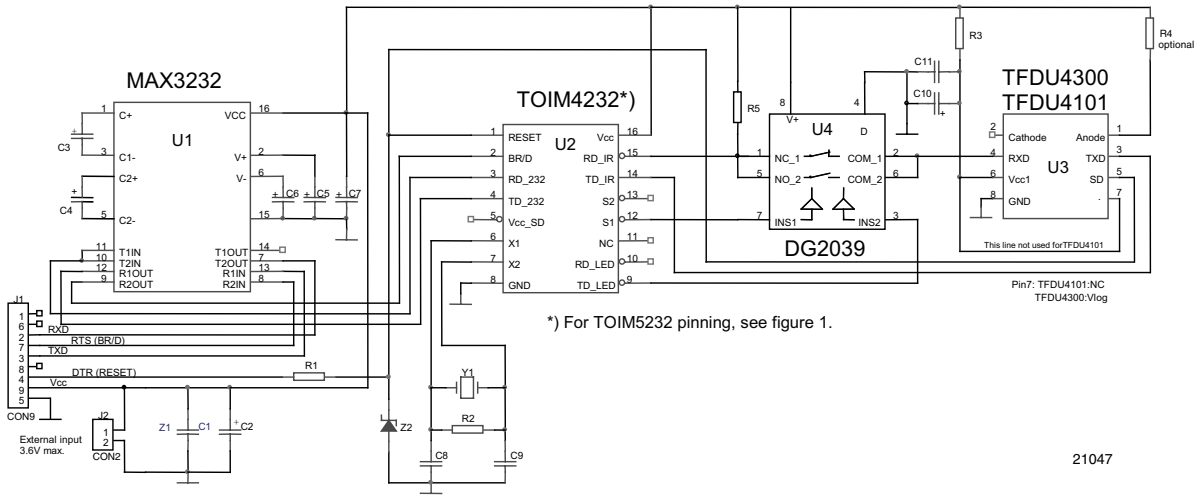


Figure 10. Demo Board Circuit with Echo-Suppression to be Used for Echo-On and Echo-Off Transceivers.

Additionally, with the programmable output S1 of the Endec the echo suppression feature can be switched on and off for testing. The default mode is echo-off. To enable the echo, S1 is to be set inactive/low. (See the chapter for programming the TOIM4232/ TOIM5232).

The oscilloscope diagrams are shown in figure 11. Channel 2 shows the echo signal on the RXD output of the TFDU4101 transceiver during transmission (Note: TFDU4300 is an echo-off design and would not show this).

Channel 1 is the signal used for gating the path from the transceiver RXD output to the Endec. On channel 3 the signal at the input of the Endec is shown with a residual signal. Finally, the output to the RS232 port, RD_232, is clean without any noise signal.

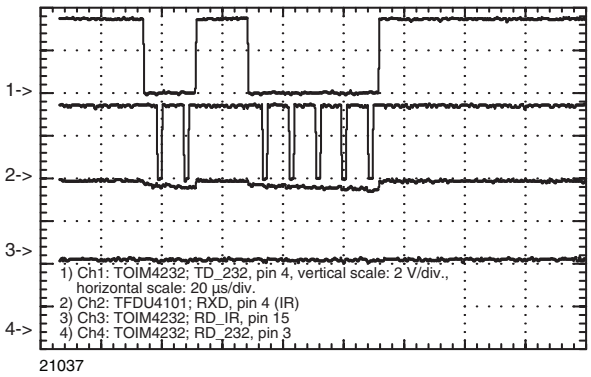


Figure 11. Echo-Suppression

For technical questions within your region, please contact one of the following:
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